Electronic Design Automation (EDA) tool development: Performance enhancements to circuit extraction

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Background

- Very Large Scale Integration (VLSI) Layout Tool
- Open source
 - Used by universities and open source developers
- Composed of design viewer and console



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Caesar or KIC2:

- Minimal support in routing features
- Hard to change a design once loaded

Magic:

- Increased design knowledge
- Easier to modify designs

Issues

- Magic is built for smaller designs
 - Moore's Law
- Labels
 - Store information on their associated cell
 - Must be referenced by name or location
- Labels are stored in a linked list



Linked Lists

- Each node keeps reference to next
- Time complexity:
 - Search: $\mathcal{O}(n)$
 - Insertion: $\mathcal{O}(1)$
 - Deletion: $\mathcal{O}(n)$



Solution

Hash Table

- Hash algorithm sorts items by index
 - Collisions resolved through chaining
- Time complexity:
 - Search: *O*(1)
 - Insertion: $\mathcal{O}(1)$
 - Deletion: $\mathcal{O}(1)$



Binned Plane (bplane)

- 2D hash table
- Cells track information about labels in the region
- Labels have near equal size and spatial distribution



Methods

- Linux Perf tool used
 - Sampling rate of 100 per second
 - Generates time spent per function
- Flame graph generated
 - Gives proportion of time spent on given function

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- 1. striVe chip loaded into Magic
- 2. Command of interest is run
- 3. Performance measured at 100 samples per second
- 4. Magic is recompiled with optimizations
- 5. Performance measured at 100 samples per second
- 6. Flame graph generated for analysis

Based on previous experience in loading large designs Chosen Areas:

- Extraction
- Net Selection
- Label Search by Content

Areas of Optimization

- extract all command extracts into .ext file
- Functions were found to be searching all labels
- plane added to CellDef
 - Properties for the cell, includes label storage
- extSubtreeFunc and extHierConnections found to be of concern

- select clear used to analyze
- DBTreeSrLabels found to take most time
- TF_LABEL_ATTACH and TF_LABEL_DISPLAY flags for labels
 - Requires use of bplane and linked list

- select short command used for profiling
 - Used because it relies on label names
- Hash table added to CellDef
- Hash table iteration implemented in DBCheckLabelsByContent

Results

Extraction



Extraction



Net Selection



Net Selection



- Perf did not detect content searching function
 - Sampling rate of 30,000 samples per second
- Confirmed to run using gdb
- Original complexity was $\mathcal{O}(n)$
 - Likely to not detect \$\mathcal{O}(1)\$

Conclusions

- General decrease in time spent on functions
- Added overhead in extraction
 - Added class initialization for bplane
- Net selection may not have been fully tested with striVe

- Use a wider variety of chips
 - Designs used might not test all cases
- Improve profiling
 - Profiling is manually stopped

Thank you to Mr. Edwards for pointing me in the right direction for optimizations and providing feedback.

Thank you to my teachers and friends.

